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EXAMINER	
SONG, JASMINE	
ART UNIT	PAPER NUMBER
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	03/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	**Application No.** 10/807,648	**Applicant(s)** SIH ET AL.	
	Examiner Jasmine Song	**Art Unit** 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,8,10-18 and 35-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-8,10-18,35--54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Detailed Action

1. This office action is in response to Amendment filed 11/22/2006, claims 6,9,19-34 have been cancelled, claims 35-54 are newly added claims. All rejections and objections not explicitly repeated below are withdrawn.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance. Applicant clearly indicated the subject matter in Fig.1 is conventional, see specification section 0013 and

0023.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 36-37 and 47-48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 36 recites the limitation "the cache controller" in line 3. There is insufficient antecedent basis for this limitation in the claim. Claim 37 is also rejected since it depended on the rejected claim 36.

Claim 47 recites the limitation "the cache controller" in line 3 and "the DME controller" in line 2. There are insufficient antecedent basis for this limitation in the claim.

Claim 48 recites the limitation "the plurality of DMA channels" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-5,7,10-13,35,38-40,43-46,49 and 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Volpe et al., US 6,895,475 B2, in view of Bourekas et al., US 6,128,703.

Regarding claim 1, Volpe teaches an integrated circuit (IC) (it is taught as a digital signal processor in the Fig.1) comprising:

a processor core (Fig.1, processor core 10) operable to perform data processing for the integrated circuit (it is taught as execution unit 30 within the processor core 10 issues requests to L1 cache and perform a cache line full operation if there is a cache miss, col.3, lines 22-31 and 50-59);

a cache memory (it is taught as cache memory level one L1 as shown in Fig.1) operable to store data for the processor core (it is taught as a cache hit occurs when an entry in the respective cache memory matches the address of the request sent out by the processor; col.3, lines 50-54); and

an on-chip memory (it is taught as a prefetch buffer as shown in Fig.3) operable to store data for the cache memory (it is taught as the read data from the speculative read is stored in prefetch buffer 260, col.5, lines 38-39), wherein the cache memory is filled with data from the on-chip memory for cache misses (it is taught as prefetch buffer is accessed in the subsequent cache line fill operation and data from the prefetch buffer starts being returned to cache memory and the core processor if there is a full prefetch buffer hit; col.5, lines 43-49 and col.10,lines 34-53), and wherein the on-chip memory is filled with data from an external memory (col.4, lines 35-39 and col.5, lines 35-39, an external memory is taught as off-chip memory 72).

Volpe does not clearly and specifically teaches that the on-chip memory is selectably filled with data from an external memory independent of the cache misses under user control. Volpe only teaches the data from the external memory is prefetched and stored in the prefetch buffer in response to a cache line fill operation which typically starts at the address that missed in the cache memory (col.5, lines 29-39 and col.6, lines 19-20).

However, Bourekas teaches that the on-chip memory is selectably filled with data from an external memory independent of the cache misses under user control (it is taught a prefetch instruction is used by a programmer to retrieve data from the memory and place the data within the cache system so that further processor instructions that require access to the data will not have to wait on the memory to provide the data, in this case, data is the specified data, see col.4, lines 56-58 and lines 62-65, also, in this case, cache memory can be considered as the second level cache memory which has the same functionality of the prefetch buffer in the Volpe, they both store the data retrieved from the main memory and supply the data to the level one cache memory; col.7, lines 61-65 and col.8, lines 65 to col.9, lines 2 and col.9, lines 7-12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Bourekas into Volpe's cache system such as the on-chip memory is selectably filled with data from an external memory independent of the cache misses under user control because a prefetch instruction which specifies an ignore hit operation can prevent the microprocessor from retrieving stale data from the cache even when a hit occurs, and the microprocessor does not

need to flush the cache or invalidate a portion of the cache memory to insure coherency between the cache memory and the main memory (see Bourekas, col.5, lines 23-29 and lines 58-64 and col.6, lines 24-30,col.9,lines 7-15 and col.10, lines 35-46).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor (both references teaches prefetching method). This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 12, Volpe teaches a wireless apparatus comprising:

Volpe teaches an integrated circuit (IC) (it is taught as a digital signal processor in the Fig.1) including:

a processor core (Fig.1, processor core 10) operable to perform data processing (it is taught as execution unit 30 within the processor core 10 issues requests to L1 cache and perform a cache line full operation if there is a cache miss, col.3, lines 22-31 and 50-59);

a cache memory (it is taught as cache memory level one L1 as shown in Fig.1) operable to store data for the processor core (it is taught as a cache hit occurs when an entry in the respective cache memory matches the address of the request sent out by the processor; col.3, lines 50-54), and

an on-chip memory (it is taught as a prefetch buffer as shown in Fig.3) operable to store data for the cache memory (it is taught as the read data from the speculative read is stored in prefetch buffer 260, col.5, lines 38-39); and an external memory

operable to store data for the on-chip memory (it is taught as data in the prefetch buffer is from the external memory; col.5, lines 35-39), wherein the cache memory is filled with data from the on-chip memory for cache misses (it is taught as prefetch buffer is accessed in the subsequent cache line fill operation and data from the prefetch buffer starts being returned to cache memory and the core processor if there is a full prefetch buffer hit; col.5, lines 43-49 and col.10,lines 34-53), and wherein the on-chip memory is filled with data from an external memory (col.4, lines 35-39 and col.5, lines 35-39, an external memory is taught as off-chip memory 72).

Volpe does not clearly and specifically teaches that the on-chip memory is selectably filled with data from an external memory independent of the cache misses under user control. Volpe only teaches the data from the external memory is prefetched and stored in the prefetch buffer in response to a cache line fill operation which typically starts at the address that missed in the cache memory (col.5, lines 29-39 and col.6, lines 19-20).

However, Bourekas teaches that the on-chip memory is selectably filled with data from an external memory independent of the cache misses under user control (it is taught a prefetch instruction is used by a programmer to retrieve data from the memory and place the data within the cache system so that further processor instructions that require access to the data will not have to wait on the memory to provide the data, in this case, data is the specified data, see col.4, lines 56-58 and lines 62-65, also, in this case, cache memory can be considered as the second level cache memory which has the same functionality of the prefetch buffer in the Volpe, they both store the data

retrieved from the main memory and supply the data to the level one cache memory; col.7, lines 61-65 and col.8, lines 65 to col.9, lines 2 and col.9, lines 7-12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Bourekas into Volpe's cache system such as the on-chip memory is selectably filled with data from an external memory independent of the cache misses under user control because a prefetch instruction which specifies an ignore hit operation can prevent the microprocessor from retrieving stale data from the cache even when a hit occurs, and the microprocessor does not need to flush the cache or invalidate a portion of the cache memory to insure coherency between the cache memory and the main memory (see Bourekas, col.5, lines 23-29 and lines 58-64 and col.6, lines 24-30,col.9,lines 7-15 and col.10, lines 35-46).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor (both references teaches prefetching method). This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 2, Volpe teaches further comprising:

a cache controller operable to handle memory transactions for the cache memory (although Volpe does not clearly show a cache controller, the cache controller is implied in the reference since the cache controller detects a cache miss, performs a cache fill operation in response to the cache miss and generates a cache miss notification, Volpe teaches detecting a cache miss, performing a cache fill operation in response to the

cache miss, therefore, the cache controller is implied in the reference. Also see Brik et al US 6978350 B2, col.1, last line to col.2, line 5).

Regarding claim 3, Volpe teaches further comprising:

a direct memory exchange (DME) controller (Fig. 3, it is taught as SDC control logic 270) operable to handle data transfers between the on-chip memory and the external memory (col.5, lines 35-39 and col.7, lines 66 to col.8, line 1).

Regarding claim 4, Volpe teaches the DME controller further operates with the cache controller to maintain data integrity for the cache memory (it is taught as cache coherence among the different levels of memories and the request data among the different levels of memories is being synchronized, col.1, lines 59-67 and col.5, lines 38-47 and col.7, lines 27-31 teaches supplying data from the lower level memory to the prefetch buffer and supplying the data such as all the words to the cache memory and the core processor from the prefetch buffer).

Regarding claim 5, Volpe teaches further comprising:

a direct memory access (DMA) controller (Fig.1, a DMA controller 16) operable to handle storage of DMA data received via at least one DMA channel (it is taught as the DMA data received at a DMA access bus 102) to the cache memory or the on-chip memory (it is taught as the DMA access bus is coupled to the system Bus interface Unit 14 and handle the DMA data to the cache memory, Fig.1), wherein the DMA controller

further operates with the cache controller to maintain data integrity for the cache memory (it is taught as cache coherence among the different levels of memories and the request data among the different levels of memories is being synchronized, col.1, lines 59-67 and col.5, lines 38-47 and col.7, lines 27-31 teaches supplying data from the lower level memory to the prefetch buffer and supplying the data such as all the words to the cache memory and the core processor from the prefetch buffer).

Regarding claim 7, Volpe teaches further comprising:

a direct memory exchange (DME) controller (Fig. 3, it is taught as SDC control logic 270) operable to handle data transfers between the on-chip memory and the external memory (col.5, lines 35-39 and col.7, lines 66 to col.8, line 1), wherein the DME controller (SDC control logic 270) couples to the DMA controller (Fig.1, DMA controller 16, col.3, line 1) via at least one DMA channel (it is taught as DMA access bus 102, see Fig.1).

Regarding claim 10, Volpe teaches the cache memory and the on-chip memory are fabricated on same integrated circuit die (Fig.1, the integrated circuit die can be considered as DSP as shown in Fig.1 which contains the cache memory and the prefetch buffer within EBIU, also see col. 2, lines 65 to col.3,lines 16).

Regarding claim 11, Volpe teaches the cache memory (Fig.4, processor core 10 contains the cache memory can be considered as a integrated circuit die) and the on-

chip memory (SDC 204 contains the prefetch buffer can be considered as another integrated circuit die) are fabricated on different integrated circuit dies encapsulated within an IC package for the integrated circuit (processor core die and SDC die can be encapsulated within an IC package as shown in Fig.1 such as DSP integrated circuit die).

Regarding claim 13, Volpe teaches further comprising:

a direct memory access (DMA) controller (Fig.1, a DMA controller 16) operable to handle storage of DMA data received via at least one DMA channel (it is taught as the DMA data received at a DMA access bus 102) to the cache memory or the on-chip memory (it is taught as the DMA access bus is coupled to the system Bus interface Unit 14 and handle the DMA data to the cache memory, Fig.1).

Regarding claim 35, Volpe teaches the DME controller (Fig. 3, it is taught as SDC control logic 270) is selectably programmable by the user to fill the on-chip memory with data from the external memory (col.5, lines 35-39 and col.7, lines 66 to col.8, line 1) independent of the cache misses, to thereby provide the user control (see the rejection of claim 1).

Regarding claim 38, Volpe teaches the DME controller is selectably programmable by a user (see rejection of claim 1) to schedule the filling of on-chip memory with data from the external memory (col.5, lines 35-39 and col.7, lines 66 to

col.8, line 1).

Regarding claim 39, Volpe teaches the DME controller is selectably programmable by the user to control the filling of the on-chip memory with data blocks from the external memory (col.5, lines 35-39 and col.7, lines 66 to col.8, line 1) such that the user functions as an anticipatory cache controller (see rejection of claim 1, in the Bourekas, a programmer is function as a cache controller since the prefetched data is from the main memory to the cache memory).

Regarding claim 40, Volpe teaches the DME controller is selectably programmable by the user to fill the on-chip memory with data from the external memory well in advance of need by the processor core and without paging-on-demand (see rejection of claim 1, Bourekas teaches the prefetch instructions, col.7, lines 61-65).

Regarding claims 43 and 52, Volpe teaches further comprising:

means for handling data transfers between the on-chip memory and the external memory (col.5, lines 35-39 and col.7, lines 66 to col.8, line 1), said means being selectably programmable by a user to fill the on-chip memory with data from the external memory independent of the cache misses (see rejection of claims 1 and 12).

Regarding claims 44 and 53, Volpe teaches said means is programmable to page blocks of instructions and/or data (c0l.5, lines 38-40) between the on-chip memory

and the external memory (col.5, lines 35-39 and col.7, lines 66 to col.8, line 1).

Regarding claims 45 and 54, Volpe teaches said means is programmable to schedule the filling of the on-chip memory with data from the external memory (col.5, lines 35-39 and col.7, lines 66 to col.8, line 1).

Regarding claim 46, Volpe teaches further comprising:

a direct memory exchange (DME) controller (Fig. 3, it is taught as SDC control logic 270) operable to handle data transfers between the on-chip memory and the external memory (col.5, lines 35-39 and col.7, lines 66 to col.8, line 1).

Regarding claim 49, Volpe teaches the DME controller is selectably programmable by a user (see rejection of claim 1) to schedule the filling of on-chip memory with data from the external memory (col.5, lines 35-39 and col.7, lines 66 to col.8, line 1).

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Volpe et al., US 6,895,475 B2 and Bourekas et al., US 6,128,703, in view of Ramchandran., US 2004/0093479 A1.

Regarding claim 8, Volpe and Bourekas teaches the claimed invention as shown above (claim 1), Volpe further teaches an internal memory bus (it is taught as system bus interface unit 14 as shown in Fig.1, bus 14 is coupled to the prefetch buffer within

EBIU 58 and the bus 14 is also coupled to cache memory which coupled to the cache controller, bus 14 is also coupled to the DMA controller, see Fig.1) coupling the on-chip memory, the cache controller, and the DMA controller.

Volpe and Bourekas do not teach the internal memory bus has a width that is equal to a line in the cache memory. However, Ramchandran teaches that the internal memory bus has a width that is equal to a line in the cache memory (Fig.7, section 0052, lines 8-10) and the number of cache lines in each cache memory is equal to the number of data buses (section 0052).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Ramchandran into Bourekas and Volpe's' cache memory system such as the memory bus width is equal to a cache line because this allows matrix transpose operations to be performed efficiently (see Ramchandran, section 0051, last two lines, also see Cassidy US 5,459,742, col.6, lines 45-50 teaches that it is preferable if a single read request on the bus will function as a cache fill, replacing an entire cache line in one operation).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

9. Claims 41-42 and 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Volpe et al., US 6,895,475 B2 and Bourekas et al., US 6,128,703, in

view of Kreitzer., US 2005/0025315 A1.

Regarding claims 41 and 50, Volpe and Bourekas teach the claimed invention as shown above (claims 1 and 12), Volpe and Bourekas do not teach said integrated circuit is operable in a wireless device, said wireless device comprising an antenna to wirelessly communicate signals with a remote base station; a receiver unit operably connected to said antenna and said integrated circuit to communicate a received signal from said antenna to said integrated circuit and a transmitter unit operably connected to said antenna and said integrated circuit to communicated data from said integrated circuit to said antenna as a transmission signal. However, Kreitzer teaches said integrated circuit (cache memory, memory 32 and processor/controller) is operable in a wireless device (Fig.1), said wireless device comprising an antenna (Fig.1, the combination of antenna 40 and 46) to wirelessly communicate signals with a remote base station; a receiver unit (Fig.1, receiver 44) operably connected to said antenna and said integrated circuit to communicate a received signal from said antenna to said integrated circuit and a transmitter unit (Fig.1, transmitter 38) operably connected to said antenna and said integrated circuit to communicated data from said integrated circuit to said antenna as a transmission signal (Fig.1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Kreitzer into Bourekas and Volpe's' memory system such as the integrated circuit is operable in a wireless device and the wireless device comprising the antenna, receiver and transmitter because it provides a secure communications in a multi-mode portable communication device and avoids

unnecessary key exchanges and reduces or eliminated set-up delays when two portable communication devices already have an established secure link and the devices can operate in multiple modes (see section 0005 and section 0006 and 0010, of Kreitzer).

Regarding claims 42 and 51, Volpe and Bourekas teaches the claims 1 and 12, Kreitzer further teaches means for communicating data between said integrated circuit and a remote base station (Fig.1, it is taught as a portable communication device such as a cellular phone is operable with a integrated circuit).

10. Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Volpe et al., US 6,895,475 B2, in view of Bourekas et al., US 6,128,703 and further in view of Wing So., Patent number 5,987,590.

Regarding claim 14, Volpe teaches an integrated circuit (it is taught as a digital signal processor in the Fig.1) comprising:

a processor (Fig.1, processor core 10) operable to perform data processing for the integrated circuit (it is taught as execution unit 30 within the processor core 10 issues requests to L1 cache and perform a cache line full operation if there is a cache miss, col.3, lines 22-31 and 50-59) and including

a processor core (Fig.1, execution unit 30) operable to perform the data processing, and

a first cache memory (it is taught as cache memory level one L1 as shown

in Fig.1) operable to store data for the processor core (it is taught as a cache hit occurs when an entry in the respective cache memory matches the address of the request sent out by the processor; col.3, lines 50-54);

an on-chip memory (it is taught as a prefetch buffer as shown in Fig.3) operable to store data for the first cache memory (it is taught as the read data from the speculative read is stored in prefetch buffer 260, col.5, lines 38-39), wherein the first cache memory is filled with data from the on-chip memory for cache misses (it is taught as prefetch buffer is accessed in the subsequent cache line fill operation and data from the prefetch buffer starts being returned to cache memory and the core processor if there is a full prefetch buffer hit; col.5, lines 43-49 and col.10,lines 34-53), and wherein the on-chip memory is filled with data from an external memory (col.4, lines 35-39 and col.5, lines 35-39, an external memory is taught as off-chip memory 72); and

a first memory bus (it is taught as system bus interface unit 14) coupling the processor to the external memory (see Fig.1).

Volpe does not clearly and specifically teaches that the on-chip memory is selectably filled with data from an external memory independent of the cache misses under user control. Volpe only teaches the data from the external memory is prefetched and stored in the prefetch buffer in response to a cache line fill operation which typically starts at the address that missed in the cache memory (col.5, lines 29-39 and col.6, lines 19-20).

However, Bourekas teaches that the on-chip memory is selectably filled with data from an external memory independent of the cache misses under user control (it is

taught a prefetch instruction is used by a programmer to retrieve data from the memory and place the data within the cache system so that further processor instructions that require access to the data will not have to wait on the memory to provide the data, in this case, data is the specified data, see col.4, lines 56-58 and lines 62-65, also, in this case, cache memory can be considered as the second level cache memory which has the same functionality of the prefetch buffer in the Volpe, they both store the data retrieved from the main memory and supply the data to the level one cache memory; col.7, lines 61-65 and col.8, lines 65 to col.9, lines 2 and col.9, lines 7-12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Bourekas into Volpe's cache system such as the on-chip memory is selectably filled with data from an external memory independent of the cache misses under user control because a prefetch instruction which specifies an ignore hit operation can prevent the microprocessor from retrieving stale data from the cache even when a hit occurs, and the microprocessor does not need to flush the cache or invalidate a portion of the cache memory to insure coherency between the cache memory and the main memory (see Bourekas, col.5, lines 23-29 and lines 58-64 and col.6, lines 24-30,col.9,lines 7-15 and col.10, lines 35-46).

Wing So teaches an integrated circuit includes a first processor operable to perform general-purpose processing for the integrated circuit and Wing So also teaches a DSP microprocessor (col.14, lines 6-14 and col.28, lines 30-36).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Wing So in the system of Volpe,

Bourekas such as an integrated circuit includes a first processor operable to perform general-purpose processing and an integrated circuit includes a DSP microprocessor because performance of the computer system is increased since the DSP microprocessor executes the CPU microprocessor operation when CPU microprocessor is too occupied. Also, multiple waiting states are avoided and the blazing DSP operation speed does not come to a halt when interfaced to the CPU (see abstract of Wing).

Regarding claim 15, Volpe teaches the second processor further includes a second cache memory operable to store instructions for the processor core (it is taught as L2 cache memory), and wherein the second cache memory is automatically filled with instructions from the on-chip memory for cache misses (col.1, lines 48-50).

Regarding claim 16, Volpe teaches the second processor further includes

a first cache controller operable to handle memory transactions for the first cache memory and a second cache controller operable to handle memory transactions for the second cache memory (although Volpe does not clearly show the cache controllers, the cache controllers are implied in the reference since the cache controllers such as L1 cache controller and L2 cache controller detect a cache miss, perform a cache fill operation in response to the cache miss and generate a cache miss notification, Volpe teaches detecting a cache miss, performing a cache fill operation in response to the cache miss, therefore, the cache controllers are implied in the reference. Also see Brik et al US 6978350 B2, col.1, last line to col.2, line 5).

a direct memory access (DMA) controller (Fig.1, a DMA controller 16) operable to handle storage of DMA data received via at least one DMA channel (it is taught as the DMA data received at a DMA access bus 102) to the cache memory or the on-chip memory (it is taught as the DMA access bus is coupled to the system Bus interface Unit 14 and handle the DMA data to the cache memories such as L1 and L2 cache, Fig.1), and

a direct memory exchange (DME) controller (Fig. 3, it is taught as SDC control logic 270) operable to handle data transfers between the on-chip memory and the external memory (col.5, lines 35-39 and col.7, lines 66 to col.8, line 1).

Regarding claim 17, Volpe teaches the DMA controller and the DME controller further operate with the first and second cache controllers to maintain data integrity for the first and second cache memories (it is taught as cache coherence among the different levels of memories and the request data among the different levels of memories is being synchronized, col.1, lines 59-67 and col.5, lines 38-47 and col.7, lines 27-31 teaches supplying data from the lower level memory to the prefetch buffer and supplying the data such as all the words to the cache memories such as L2 cache and L1 cache and the core processor from the prefetch buffer).

Regarding claim 18, Volpe teaches the second processor further includes a second memory bus (it is taught as external access bus, see Fig.1) coupling the on-chip memory (prefetch buffer within EBIU 58), the first and second cache controllers (L1 and

L2 controllers within or connected to the both caches), and the DMA controller (DMA controller 16), and wherein the DME controller couples to the DMA controller via at least one DMA channel (see Fig.1).

Response to Applicant's Arguments

11. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

14. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 7:30-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jasmine Song

Jasmine Song

Patent Examiner 3/2/07

March 2, 2007